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EXAMINER	
TORRES, JOSEPH D	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 07/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/777,213	BETTS, WILLIAM L.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28,31-38,50-57 and 90-93* is/are pending in the application.

4a) Of the above claim(s) *16-28 and 91* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15,31-38,50-57,90,92 and 93* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 February 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *20050617*.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1-15, 31-38, 50-57, 90, 92 and 93, drawn to A generalized convolution encoder comprised of a plurality of computational elements for adaptively adjusting the constraint length of the convolutional code, classified in class 714, subclass 774.

   II. Claims 16-28 and 91, drawn to A generalized convolution encoder comprised of a plurality of convolutional encoders, classified in class 714, subclass 786.

The inventions are distinct, each from the other because of the following reasons: Inventions Group I and Group II are unrelated. Inventions are unrelated if it can be shown that they are not disclosed as capable of use together and they have different modes of operation, different functions, or different effects (MPEP § 806.04, MPEP § 808.01). In the instant case the invention of Group II generates a generalized convolution code by using a different function or mode of operation, that is the generalized convolution code is generated using a plurality of convolutional encoders whereas the invention of Group I generates a generalized convolution code by using a different computational function or computational mode of operation.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group II is not required for Group I, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art because of their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

During a telephone conversation with Karen Hazzah on 6/17/2005 a provisional election was made without traverse to prosecute the invention of Group I, claims 1-15, 31-38, 50-57, 90, 92 and 93. Affirmation of this election must be made by applicant in replying to this Office action. Claims 16-28 and 91 withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Response to Arguments

2. Applicant's arguments with respect to claims 1-15, 31-38, 50-57, 90, 92 and 93 have been considered but are moot in view of the new ground(s) of rejection.

Specification

3. The disclosure is objected to because of the following informalities:

4. Claim 31 recites, "A system for encoding information", in the preamble. The Examiner asserts that modulation or encryption coding are also systems for encoding. The Applicant does not teach anywhere in the specification the system recited in the body of claim 31 for modulation or encryption coding, but instead only teaches the system recited in the body of claim 31 for interleaved generalized convolutional encoding.

A system as in claim 31 for modulation or encryption coding critical or essential to the practice of the invention, but not included in the claim(s) is not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976).

Claim 50 recites, "A computer readable medium for encoding information", in the preamble. The Examiner asserts that modulation or encryption coding are also systems for encoding. The Applicant does not teach anywhere in the specification the system recited in the body of claim 31 for modulation or encryption coding, but instead only teaches the system recited in the body of claim 50 for interleaved generalized convolutional encoding.

A computer readable medium as in claim 50 for modulation or encryption coding critical or essential to the practice of the invention, but not included in the claim(s) is not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976).

The Examiner would also like to point out that there are 52,236 patents, applications and foreign documents using the terms "encoder and (delay flip-flop latch (shift adj register))" in a EAST search. Even if it were possible for EAST to pull all 52,236 patents, applications and foreign documents in a single session, the Examiner has not intention of searching all of the patents since the Examiner is only qualified to examine patents in error correction. Even if the Examiner gave up out of frustration and allowed the claims to get the patent out of the Examiner's hair and to avoid a search of 52,236 patents, applications and foreign documents, the Examiner would have to make a record of the Examiner's frustration at the time of allowance, which the Examiner does not believe would lend itself to creating confidence in the industry of a valid patent. This is unfortunate because the Examiner does recognize the novelty of the convolutional encoding and interleaving structure of Figure 5 in the Applicant's disclosure that controls the depth of the delay elements between taps to produce convolutionally encoded and interleaved sequences. The Examiner suggests that the Applicant claim the Applicant's invention as taught in the Applicant's specification and the Applicant's Figures 5 and 6. Appropriate correction is required.

Claim 1 recites, "the plurality of logic calculators generating an output **based on** the data input, the plurality of prior data inputs, the plurality of logic calculators, and the time delay" [Emphasis Added]. The Examiner would like to point out that the Applicant does not teach every conceivable combination of logic calculators for generating an output **based on** data input, a plurality of prior data inputs, a plurality of logic calculators, and a time delay and it is not clear that every combination of logic calculators for generating an output **based on** data input, a plurality of prior data inputs, a plurality of logic calculators, and a time delay has any useful utility. The Applicant only teaches a one embodiments exemplified by the Applicant's Figure 5-6.

Claim 31 recites, "fifth means for producing an output, wherein the output is **based on** the operation of the first means, the second means, the third means, and the fourth means" [Emphasis Added]. The Examiner would like to point out that the Applicant does not teach every conceivable combination of logic calculators for generating an output **based on** data input, a plurality of prior data inputs, a plurality of logic calculators, and a time delay and it is not clear that every combination of logic calculators for generating an output **based on** data input, a plurality of prior data inputs, a plurality of logic calculators, and a time delay has any useful utility. The Applicant only teaches a one embodiments exemplified by the Applicant's Figure 5-6.

Claim 50 recites, "logic for producing an output, the output being **based on** the operation of the logic for receiving a data input, the logic for delaying a plurality of prior data inputs, the logic for storing the delayed plurality of prior data inputs, and the logic for performing logic calculations" [Emphasis Added]. The Examiner would like to point

out that the Applicant does not teach every conceivable combination of logic calculators for generating an output **based on** data input, a plurality of prior data inputs, a plurality of logic calculators, and a time delay and it is not clear that every combination of logic calculators for generating an output **based on** data input, a plurality of prior data inputs, a plurality of logic calculators, and a time delay has any useful utility. The Applicant only teaches a one embodiments exemplified by the Applicant's Figure 5-6.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 31-38, 50-57, 92 and 93 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure, which is not enabling. Claim 31 recites, "A system for encoding information", in the preamble. The Examiner asserts that modulation or encryption coding are also systems for encoding. The Applicant does not teach anywhere in the specification the system recited in the body of claim 31 for modulation or encryption coding, but instead only teaches the system recited in the body of claim 31 for interleaved generalized convolutional encoding.

A system as in claim 31 for modulation or encryption coding critical or essential to the practice of the invention, but not included in the claim(s) is not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976).

Claim 50 recites, "A computer readable medium for encoding information", in the preamble. The Examiner asserts that modulation or encryption coding are also systems for encoding. The Applicant does not teach anywhere in the specification the system recited in the body of claim 31 for modulation or encryption coding, but instead only teaches the system recited in the body of claim 50 for interleaved generalized convolutional encoding.

A computer readable medium as in claim 50 for modulation or encryption coding critical or essential to the practice of the invention, but not included in the claim(s) is not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976).

The Examiner would also like to point out that there are 52,236 patents, applications and foreign documents using the terms "encoder and (delay flip-flop latch (shift adj register))" in a EAST search. Even if it were possible for EAST to pull all 52,236 patents, applications and foreign documents in a single session, the Examiner has not intention of searching all of the patents since the Examiner is only qualified to examine patents in error correction. Even if the Examiner gave up out of frustration and allowed the claims to get the patent out of the Examiner's hair and to avoid a search of 52,236 patents, applications and foreign documents, the Examiner would have to make a record of the Examiner's frustration at the time of allowance, which the Examiner does not believe would lend itself to creating confidence in the industry of a valid patent. This is unfortunate because the Examiner does recognize the novelty of the convolutional encoding and interleaving structure of Figure 5 in the Applicant's disclosure that controls

the depth of the delay elements between taps to produce convolutionally encoded and interleaved sequences. The Examiner suggests that the Applicant claim the Applicant's invention as taught in the Applicant's specification and the Applicant's Figures 5 and 6.

Claims 1-15, 31-38, 50-57, 90, 92 and 93 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 1 recites, "the plurality of logic calculators generating an output **based on** the data input, the plurality of prior data inputs, the plurality of logic calculators, and the time delay" [Emphasis Added]. The Examiner would like to point out that the Applicant does not teach every conceivable combination of logic calculators for generating an output **based on** data input, a plurality of prior data inputs, a plurality of logic calculators, and a time delay and it is not clear that every combination of logic calculators for generating an output **based on** data input, a plurality of prior data inputs, a plurality of logic calculators, and a time delay has any useful utility. The Applicant only teaches a one embodiments exemplified by the Applicant's Figure 5-6.

Claim 31 recites, "fifth means for producing an output, wherein the output is **based on** the operation of the first means, the second means, the third means, and the fourth means" [Emphasis Added]. The Examiner would like to point out that the Applicant does not teach every conceivable combination of logic calculators for generating an

output **based on** data input, a plurality of prior data inputs, a plurality of logic calculators, and a time delay and it is not clear that every combination of logic calculators for generating an output **based on** data input, a plurality of prior data inputs, a plurality of logic calculators, and a time delay has any useful utility. The Applicant only teaches a one embodiments exemplified by the Applicant's Figure 5-6.
Claim 50 recites, "logic for producing an output, the output being **based on** the operation of the logic for receiving a data input, the logic for delaying a plurality of prior data inputs, the logic for storing the delayed plurality of prior data inputs, and the logic for performing logic calculations" [Emphasis Added]. The Examiner would like to point out that the Applicant does not teach every conceivable combination of logic calculators for generating an output **based on** data input, a plurality of prior data inputs, a plurality of logic calculators, and a time delay and it is not clear that every combination of logic calculators for generating an output **based on** data input, a plurality of prior data inputs, a plurality of logic calculators, and a time delay has any useful utility. The Applicant only teaches a one embodiments exemplified by the Applicant's Figure 5-6.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-15, 31-38, 50-57, 90, 92 and 93 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. Claim 1 recites, "A interleaved generalized convolutional encoder", in the preamble. The omitted elements

are: any relationship between the elements of the body of the claim and the "interleaved generalized convolutional encoder". That is one would expect an interleaved generalized convolutional encoder to accept some data input and to generate from the data input, an interleaved convolutionally encoded data stream. There is no indication in the body of the claim language that any interleaved convolutionally encoded data stream is produced from the data input.

Claim 31 recites, "A system for encoding information", in the preamble. The omitted elements are: any relationship between the elements of the body of the claim and the "system for encoding information". That is one would expect a system for encoding information to accept some data input and to generate from the data input, an encoded data stream. There is no indication in the body of the claim language that any encoded data stream is produced from the data input.

Claim 50 recites, "A computer readable medium for encoding information", in the preamble. The omitted elements are: any relationship between the elements of the body of the claim and the "computer readable medium for encoding information". That is one would expect a computer readable medium for encoding information to accept some data input and to generate from the data input, an encoded data stream. There is no indication in the body of the claim language that any encoded data stream is produced from the data input.

The Examiner would also like to point out that there are 52,236 patents, applications and foreign documents using the terms "encoder and (delay flip-flop latch (shift adj register))" in a EAST search (Note: since encoder only appears in the preamble, the

examiner does not even have to give patentable weight to encoder). Even if it were possible for EAST to pull all 52,236 patents, applications and foreign documents in a single session, the Examiner has not intention of searching all of the patents since the Examiner is only qualified to examine patents in error correction. Even if the Examiner gave up out of frustration and allowed the claims to get the patent out of the Examiner's hair and to avoid a search of 52,236 patents, applications and foreign documents, the Examiner would have to make a record of the Examiner's frustration at the time of allowance, which the Examiner does not believe would lend itself to creating confidence in the industry of a valid patent. This is unfortunate because the Examiner does recognize the novelty of the convolutional encoding and interleaving structure of Figure 5 in the Applicant's disclosure that controls the depth of the delay elements between taps to produce convolutionally encoded and interleaved sequences. The Examiner suggests that the Applicant claim the Applicant's invention as taught in the Applicant's specification and the Applicant's Figures 5 and 6.

Claims 1-15, 31-38, 50-57, 90, 92 and 93 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites, "one of a stream of data symbols". It is not clear what "one of" refers to since there is only one stream recited after the term "one of". The Examiner assumes the Applicant simply intended: --a stream of data symbols-- since a stream of data symbols is substantially "one of a stream of data symbols".

The term "prior data inputs" in claim 1 is a relative term which renders the claim indefinite. The term "prior data inputs" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. The term "prior" implies that prior data inputs are data used in some prior event. Since no event is cited to gauge the relative placement in time of any prior data input, the Examiner assumes that the Applicant intended --data inputs-- in place of "prior data inputs".

Claim 1 recites, "the plurality of logic calculators generating an output **based on** the data input, the plurality of prior data inputs, the plurality of logic calculators, and the time delay" [Emphasis Added]. The term "based on" is indefinite since it does not set forth the relationship between "the plurality of logic calculators" and "the data input, the plurality of prior data inputs, the plurality of logic calculators, and the time delay".

Claim 1 recites, "the memory element being capable of storing a plurality of prior data inputs". The Term "capable of" is indefinite (Note: shift registers are always capable of storing data whether they actually sore data or not).

Claim 31 recites, "one of a stream of data symbols". It is not clear what "one of" refers to since there is only one stream recited after the term "one of". The Examiner assumes the Applicant simply intended: --a stream of data symbols-- since a stream of data symbols is substantially "one of a stream of data symbols".

The term "prior data inputs" in claim 31 is a relative term which renders the claim indefinite. The term "prior data inputs" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary

skill in the art would not be reasonably apprised of the scope of the invention. The term "prior" implies that prior data inputs are data used in some prior event. Since no event is cited to gauge the relative placement in time of any prior data input, the Examiner assumes that the Applicant intended --data inputs-- in place of "prior data inputs".

Claim 31 recites, "fifth means for producing an output, wherein the output is **based on** the operation of the first means, the second means, the third means, and the fourth means" [Emphasis Added]. The term "based on" is indefinite since it does not set forth the relationship between "the plurality of logic calculators" and "the data input, the plurality of prior data inputs, the plurality of logic calculators, and the time delay".

Claim 50 recites, "one of a stream of data symbols". It is not clear what "one of" refers to since there is only one stream recited after the term "one of". The Examiner assumes the Applicant simply intended: --a stream of data symbols-- since a stream of data symbols is substantially "one of a stream of data symbols".

The term "prior data inputs" in claim 50 is a relative term which renders the claim indefinite. The term "prior data inputs" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. The term "prior" implies that prior data inputs are data used in some prior event. Since no event is cited to gauge the relative placement in time of any prior data input, the Examiner assumes that the Applicant intended --data inputs-- in place of "prior data inputs".

Claim 50 recites, "logic for producing an output, the output being **based on** the operation of the logic for receiving a data input, the logic for delaying a plurality of prior

data inputs, the logic for storing the delayed plurality of prior data inputs, and the logic for performing logic calculations" [Emphasis Added]. The term "based on" is indefinite since it does not set forth the relationship between "the plurality of logic calculators" and "the data input, the plurality of prior data inputs, the plurality of logic calculators, and the time delay".

Claims 1-15, 31-38, 50-57, 90, 92 and 93 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. Claim 1 recites, "the plurality of logic calculators generating an output **based on** the data input, the plurality of prior data inputs, the plurality of logic calculators, and the time delay" [Emphasis Added]. The omitted structural cooperative relationships are: the relationship between "the plurality of logic calculators" and "the data input, the plurality of prior data inputs, the plurality of logic calculators, and the time delay".

Claim 31 recites, "fifth means for producing an output, wherein the output is **based on** the operation of the first means, the second means, the third means, and the fourth means" [Emphasis Added]. The omitted structural cooperative relationships are: the relationship between "fifth means for producing an output" and "the operation of the first means, the second means, the third means, and the fourth means".

Claim 50 recites, "logic for producing an output, the output being **based on** the operation of the logic for receiving a data input, the logic for delaying a plurality of prior

data inputs, the logic for storing the delayed plurality of prior data inputs, and the logic for performing logic calculations" [Emphasis Added]. The omitted structural cooperative relationships are: the relationship between "the plurality of logic calculators" and "the data input, the plurality of prior data inputs, the plurality of logic calculators, and the time delay".

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

7. Claims 1-15, 31-38, 50-57, 90, 92 and 93 are rejected under 35 U.S.C. 101 because the claimed invention lacks patentable utility. Claim 1 recites, "the plurality of logic calculators generating an output **based on** the data input, the plurality of prior data inputs, the plurality of logic calculators, and the time delay" [Emphasis Added]. The Examiner would like to point out that the Applicant does not teach every conceivable combination of logic calculators for generating an output **based on** data input, a plurality of prior data inputs, a plurality of logic calculators, and a time delay and it is not clear that every combination of logic calculators for generating an output **based on** data input, a plurality of prior data inputs, a plurality of logic calculators, and a time delay has any useful utility. The Applicant only teaches a one embodiments exemplified by the Applicant's Figure 5-6.

Claim 31 recites, "fifth means for producing an output, wherein the output is **based on** the operation of the first means, the second means, the third means, and the fourth

means" [Emphasis Added]. The Examiner would like to point out that the Applicant does not teach every conceivable combination of logic calculators for generating an output **based on** data input, a plurality of prior data inputs, a plurality of logic calculators, and a time delay and it is not clear that every combination of logic calculators for generating an output **based on** data input, a plurality of prior data inputs, a plurality of logic calculators, and a time delay has any useful utility. The Applicant only teaches a one embodiments exemplified by the Applicant's Figure 5-6.
Claim 50 recites, "logic for producing an output, the output being **based on** the operation of the logic for receiving a data input, the logic for delaying a plurality of prior data inputs, the logic for storing the delayed plurality of prior data inputs, and the logic for performing logic calculations" [Emphasis Added]. The Examiner would like to point out that the Applicant does not teach every conceivable combination of logic calculators for generating an output **based on** data input, a plurality of prior data inputs, a plurality of logic calculators, and a time delay and it is not clear that every combination of logic calculators for generating an output **based on** data input, a plurality of prior data inputs, a plurality of logic calculators, and a time delay has any useful utility. The Applicant only teaches a one embodiments exemplified by the Applicant's Figure 5-6.

8. Claims 31-38, 50-57, 92 and 93 rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claims 31 and 50 recite abstract algorithms that can be carried out by hand or by a computer program with no

tangible connection to any hardware. Computer programs are non-statutory. Abstract algorithms are non-statutory.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. Claims 1, 5-7, 10, 31, 34, 35, 38, 50, 53, 54, 57, 90, 92 and 93 are rejected under 35 U.S.C. 103(a) as being unpatentable over Davis; Robert C. (US 4545054 A) in view of Sinha; Deepen et al. (US 6223324 B1, hereafter referred to as Sinha).

35 U.S.C. 103(a) rejection of claims 1, 31, 50, 90, 92 and 93.

Davis teaches a node, the node being capable of receiving a data input, the data input being a portion of one of a stream of data symbols (Input 10 of Figure 1 in Davis inputs data to a node of a convolutional encoder);

a memory element, the memory element being capable of storing a plurality of prior data inputs (Encoder Shift Register Element 11 in Figure 1 of Davis is a memory element, the memory element being capable of storing a plurality of prior data inputs), and outputting the plurality of prior data inputs after a time delay having a value M, where M is configurable to a first value (M=n in Figure 1 of Davis; Note: Davis teaches that n=M is configurable to produce a specific convolutional code based on the generator polynomial of the convolutional code); and

a plurality of logic calculators (Adders 12 and 13 in Figure 1 of Davis are a plurality of logic calculators), the plurality of logic calculators generating an output based on the data input, the plurality of prior data inputs, the plurality of logic calculators, and the time delay (Adders 12 and 13 in Figure 1 of Davis generate an output based on the data input, the plurality of prior data inputs, the plurality of logic calculators, and the time delay).

However Davis does not explicitly teach the specific use of run-time to a first value configuration of the delay M.

Sinha, in an analogous art, teaches that different convolutional codes are used for different bits and the decision to use different convolutional codes is made at run-time (see Abstract in Sinha).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Davis with the teachings of Sinha by including use of run-time to a first value configuration of the delay M. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because

one of ordinary skill in the art would have recognized that use of run-time to a first value configuration of the delay M would have provided unequal error protection for transmission data (see Abstract in Sinha).

35 U.S.C. 103(a) rejection of claim 5.

Figure 1 of Davis teaches that the time delay is a plurality of unit time delays.

35 U.S.C. 103(a) rejection of claims 6, 34 and 53.

The receiver in Sinha determines the amount of convolutional encoding, hence sets the delay.

35 U.S.C. 103(a) rejection of claims 7, 35 and 54.

The receiver in Sinha determines the amount of convolutional encoding, hence sets the delay.

35 U.S.C. 103(a) rejection of claims 10, 38 and 57.

Set n=3 in Figure of Davis. That is the Davis patent encompasses a delay of 3 baud as a specific embodiment of Figure 1 in Davis.

10. Claims 2-4, 11-15, 32, 33, 51 and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Davis; Robert C. (US 4545054 A) and Sinha; Deepen et al.

(US 6223324 B1, hereafter referred to as Sinha) in view of Herzberg; Hanan (US 5996104 A).

35 U.S.C. 103(a) rejection of claims 2, 32 and 51.

Davis and Sinha substantially teaches the claimed invention described in claims 1, 31 and 50 (as rejected above).

However Davis and Sinha does not explicitly teach the specific use of a PAM symbol.

Herzberg, in an analogous art, teaches use of a PAM symbol (Col. 13, lines 63-67 in Herzberg teach that the data input is a portion of a PAM symbol).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Davis and Sinha with the teachings of Herzberg by including use of a PAM symbol. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a PAM symbol would have provided error protection for PAM symbols.

35 U.S.C. 103(a) rejection of claim 3.

Serial to Parallel converter 12 in Figure 1 of Herzberg is a switch for directing input to different convolutional encoders.

35 U.S.C. 103(a) rejection of claims 4, 33 and 52.

Col. 13, lines 63-67 in Herzberg teach that the data input is a portion of a PAM symbol.

35 U.S.C. 103(a) rejection of claim 11.

Binary multiplication is implemented using AND gates and binary addition using XOR gates, hence AND and XOR gates are the circuit implementation for Figure 4A in Herzberg.

35 U.S.C. 103(a) rejection of claim 12.

Symbol Selector 16 in Figure 18B in Herzberg is a mapper.

35 U.S.C. 103(a) rejection of claims 13 and 14.

Davis, Sinha and Herzberg substantially teaches the claimed invention described in claims 1-7 and 10-12 (as rejected above).

However Davis, Sinha and Herzberg do not explicitly teach the specific use of software or firmware.

The Examiner asserts that one of ordinary skill in the art at the time the invention was made would have know that firmware and software implementations provide the added benefit of flexibility and scalability.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Davis, Sinha and Herzberg by including use of software or firmware. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of software or firmware would have provided

the opportunity to implement an alternative embodiment of the teachings in Davis, Sinha and Herzberg, which was flexible and scalable.

35 U.S.C. 103(a) rejection of claim 15.

The convolutional encoder of Figure 4A in Herzberg is inherently capable of implementing the specific encoder of the Applicant's claim 15. See In re Swinehart, 439 F.2d 210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971) and In re Schreiber, 128 F.3d 1473, 1477, 44 USPQ2d 1429, 1431 (Fed. Cir. 1997).

11. Claims 8, 9, 36, 37, 55 and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Davis; Robert C. (US 4545054 A), Sinha; Deepen et al. (US 6223324 B1, hereafter referred to as Sinha) and Herzberg; Hanan (US 5996104 A) in view of Ross; Daniel P. (US 4901319 A).

35 U.S.C. 103(a) rejection of claims 8, 36 and 55.

Davis, Sinha and Herzberg substantially teaches the claimed invention described in claims 1-7, 31-35 and 50-54 (as rejected above).

However Davis, Sinha and Herzberg does not explicitly teach the specific use of the adaptive parameters based on the quality of a transmission path between a transmitter and the receiver.

Ross, in an analogous art, teaches adaptive parameters based on the quality of a transmission path between a transmitter and the receiver (se Abstract, Ross).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Herzberg and Khoury with the teachings of Ross by including use of adaptive parameters based on the quality of a transmission path between a transmitter and the receiver. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of adaptive parameters based on the quality of a transmission path between a transmitter and the receiver would have provided the opportunity to vary interleaving parameters according to transmission quality.

35 U.S.C. 103(a) rejection of claims 9, 37 and 56.

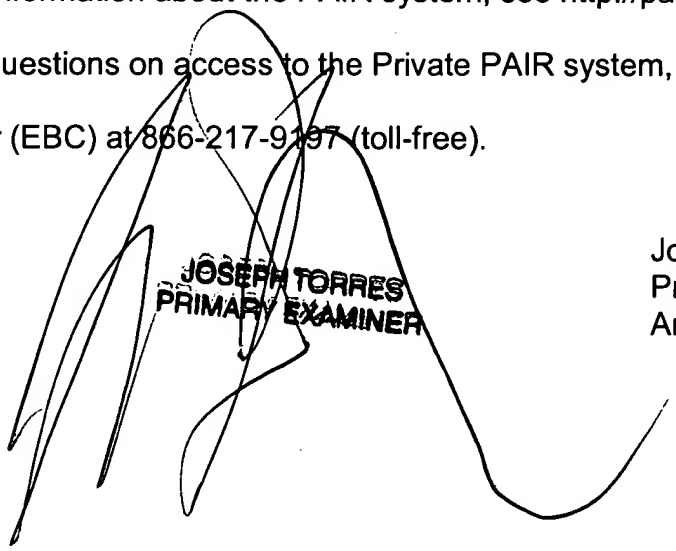
Fading is a type of noise affecting transmission quality (see Abstract in Ross).

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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